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Crystalline–Amorphous Silicon Nanocomposites with Reduced Thermal Conductivity for Bulk Thermoelectrics

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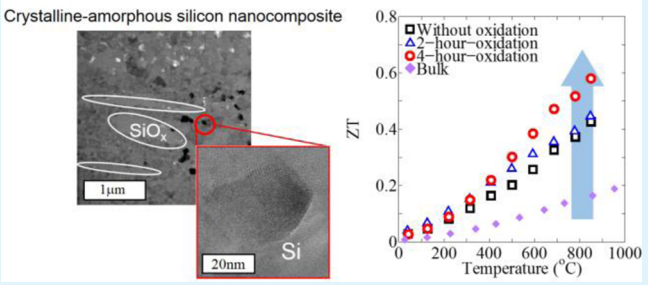
ABSTRACT: Responding to the need for thermoelectric materials with high efficiency in both conversion and cost, we developed a nanostructured bulk silicon thermoelectric materials by sintering silicon crystal quantum dots of several nanometers in diameters synthesized by plasma-enhanced chemical vapor deposition (PECVD). The material consists of hybrid structures of nanograins of crystalline silicon and amorphous silicon oxide. The percolated nanocrystalline region gives rise to high power factor with the high doping concentration realized by PECVD, and the binding amorphous region reduces thermal conductivity. Consequently, the nondimensional figure of merit reaches 0.39 at 600 °C, equivalent to the best reported value for silicon thermoelectrics. The thermal conductivity of the densely packed material is as low as 5 W m^{-1} K^{-1} in a wide temperature range from room temperature to 1000 °C, which is beneficial not only for the conversion efficiency but also for material cost by requiring less material to establish certain temperature gradient.



KEYWORDS: *thermoelectric material, silicon, nanostructure, thermal conductivity, plasma-enhanced chemical vapor deposition, plasma activated sintering*

INTRODUCTION

Thermoelectric materials are capable of directly converting heat into electricity via Seebeck effect. Thermoelectric modules have an advantage over mechanical heat engines in harvesting energy from a ubiquitous heat source because the solid-state energy conversion enables maintenance-free operation and high output current density even with small modules. However, the use of thermoelectric modules in today's technology is limited, largely due to the poor cost efficiency of the material. Therefore, it is important not only to enhance conversion efficiency but also to reduce material cost per efficiency.

There has been a great enhancement in the conversion efficiency of thermoelectric materials over the past decade, and there are now many materials with nondimensional figure-of-merit ZT larger than 1. Here, ZT is defined as $S^2\sigma T/\kappa$, where S is the Seebeck coefficient, σ is the electrical conductivity, κ is the thermal conductivity, and T is the average absolute temperature. One approach has been to enhance the power factor ($S^2\sigma$) using for instance the large density of states near Fermi level generated by quantum confinement[1] or resonant doping,[2] 2D electron gas,[3] and energy filtering.[4] Another approach has been to reduce lattice thermal conductivity by scattering phonons with lattice anharmonicity,[5] alloys[6] and nanostructures.[7]

From a practical viewpoint, nanostructured bulk materials fabricated using a bulk process have caught great attention due to its scalability. This is typically done by hot-pressing/sintering ball-milled nanopowders or precipitating second-phase nanocrystals in a bulk matrix, and ZT enhancement has been reported for various materials such as Bi_2Te_3,[7] PbTe[8,9] and Si–Ge.[10,11] The general strategy here is to reduce lattice thermal conductivity without appreciably sacrificing carrier transport by making the nanostructures smaller than the phonon mean free path (MFP) but larger than the electron MFP.[12] The thermal reduction effect, with the recent advances in first-principles calculations, can be quantitatively understood and predicted from phonon-mode-dependent heat conduction in single crystals[13] and nanostructured bulk material.[14]

On the other hand, for energy harvesting applications such as power supply for wireless sensor networks or condition monitoring system, ZT = 1 could be sufficient if the costs of material and process were low. This is, however, not the case for most of the above high ZT materials, even for the scalable bulk materials, because of the limited abundance and premature process technology, which needs to be established for each material incorporating its chemical, thermal and mechanical properties. In this sense, silicon (Si) is an attractive candidate for its highest abundance and compatibility with the current Si technology, in addition to the absence of toxicity.

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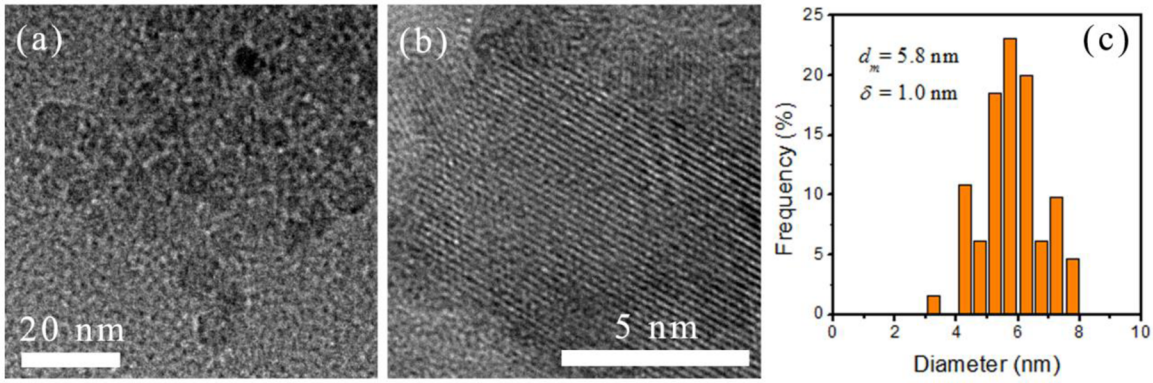

Figure 1. (a) Low-resolution TEM image, (b) typical high-resolution TEM image and (c) size distribution for the P-doped Si nanoparticles obtained from PECVD.

Although potential of crystalline Si has been known for many years,[15,16] the problem for bulk Si materials has been its high thermal conductivity. Thermal conductivity can be reduced by mechanical powdering and hot-press/sintering; however, the challenge there has been to realize homogeneous doping at high carrier concentration after high-temperature processes, and to control the state of grain boundaries that are easily oxidized. The possibility to overcome these challenges has been recently demonstrated by advances in nanostructuring techniques. Bux et al.[17] showed the reduction of thermal conductivity can be realized without appreciablely reducing the power factor by sintering nanoparticles with sizes as small as 10−100 nm made by ball-milling a very-highly doped Si crystal. As a more scalable process, Kessler et al.[18] used the plasma-enhanced chemical vapor deposition (PECVD) method to produce Si nanoparticles at 0.5 kg h^{-1}. Using the PECVD, Schierning et al.[19] studied the influence of oxygen on microstructure and transport properties of the nanocomposite and Claudio et al.[20] synthesized Si nanoparticles with grain size of 14 nm without unwanted incorporation of impurities, which resulted in preserving a high power factor.

Despite the above progresses in nanostructured bulk silicon materials, the thermal conductivity (>10 W m^{-1} K^{-1}) still remains higher than the high ZT thermoelectric materials (<10 W m^{-1} K^{-1}). The high thermal conductivity not only limits the conversion efficiency but also increases the amount of material required to establish certain temperature gradient, which results in reducing the material cost efficiency. In other words, if one can reduce thermal conductivity even without changing the conversion efficiency, the cost efficiency can be improved inverse proportionally.

In this study, we propose a hybrid material consisting of nanostructured crystalline Si and amorphous silicon oxide (SiO_x). The crystalline part serves to give rise to a high power factor, and grain boundaries and the amorphous part serves to reduce thermal conductivity. The material is realized by plasma-sintering Si/SiO_x core−shell nanoparticles with very small particle size (several nanometers) synthesized by PECVD and controlled oxidization. The promising performance of the material as a high cost-efficiency material is demonstrated by detailed characterizations of the structure and transport/conversion properties.

EXPERIMENTAL SECTION

We first synthesized Si nanoparticles by PECVD. The PECVD method has advantages in realizing doping with homogeneous distribution and high concentration. Note that even one dopant atom per particle with nanometer size results in a large doping concentration when sintered into a bulk material. The bottom-up method is also advantageous to avoid contamination, which could be problematic in the case of top-down contacting methods. Finally, the crystallite size can be tuned between a few and a few hundred nanometers, with small distribution.[21]

As for the feedstock for the PECVD, we used silicon tetrachloride ($SiCl_4$). The use of $SiCl_4$ is highly desirable because it is significantly cheaper and safer than SiH_4, which was used in prior work.[18−20] The synthesis of phosphorus (P)-doped Si nanoparticles by means of PECVD was similar to that described elsewhere.[22] About 7 standard cubic centimeters per minute (sccm) $SiCl_4$, 40 sccm trimethylphosphite ($P(OCH_3)_3$) (TMP), 70 sccm H_2 and 390 sccm Ar were introduced into the plasma system, respectively, leading to a pressure of 400 Pa. The power that coupled into the plasma for synthesizing the P-doped Si nanoparticles was maintained at 150 W. The P concentration in Si nanoparticles was determined via inductively coupled plasma mass spectroscopy (ICP-MS) (Agilent 7700x). N-type doping with 0.5 atomic percent was achieved by adding trimethyl phosphite ($P(OCH_3)_3$) to the gas.[22] With the synthesis conditions, we obtain Si nanoparticles with an average diameter of 6 nm by controlling the reaction time. Figure 1a,b shows the TEM images of the nanoparticles and their narrow size distribution.

The Si nanoparticles were next exposed to air and stirred at room temperature to oxidize the surface. During the oxidization, chlorine atoms terminating the Si nanoparticle surface is substituted by oxygen atoms.[21] The exposure time before sintering was varied from 2 to 12 h to obtain samples with different oxide-shell thicknesses.

The obtained Si/SiO_x core−shell nanoparticles were sintered by plasma activated sintering (PAS) process using Ed-PAS IV (Elenix). In the process, the temperature is controlled by DC current and the resistance heating in combination with mechanical pressure shortens the sintering time. The advantage of the PAS process is that AC current is applied to activate the particle surfaces and enhance particle sinterability before applying DC current. The sintering conditions are summarized in Table 1.

Structural characterization was carried out using transmission electron microscopy (TEM) and energy-dispersive X-ray spectroscopy (EDS) analysis. The average grain size was measured by the small-angle X-ray scattering (SAXS) using SmartLab (Rigaku).

Thermoelectric properties were characterized from room temperature up to 1000 °C. The thermal diffusivity α was measured by the laser flash method using LFA 457 (NETZSCH). The thermal conductivity κ was calculated as $\kappa = \rho C_p \alpha$, where ρ is the density of the sample measured using the Archimedes method at room temperature and C_p is the specific heat of bulk Si.[23] The electrical conductivity and Seebeck coefficient were measured on a bar-shaped sample by a direct measurement technique using ZEM-3 (ULVAC). The carrier concentration was determined at room temperature using Hall effect measurement carried out in the common Hall bar geometry

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Table 1. Sintering Conditions, Relative Densities, Average Grain Size, Carrier Concentration and Carrier Mobility[a]

oxidation time	no-oxidation	2 h	4 h	12 h
pressure (MPa)	96	96	96	96
sintering temp. (°C)	980	910	960	1000
sintering time (min)	2	1	4	2
relative density (%)	99.2	98.8	95.2	97.1
grain size (nm)	27	38	32	20
carrier concentration ($\times 10^{20}$ cm^{-3})	1.48	2.50	1.20	1.05
carrier mobility (cm^2 V^{-1} s^{-1})	9.9	19.6	18.5	0.03

[a]The properties are the values at room temperature.

with magnetic fields between −9 and +9 T using PPMS (Quantum Design).

RESULTS AND DISCUSSION

As shown in Table 1, the density of the sintered nanostructured Si samples was 95−99% compared with that of bulk single-crystalline Si. The TEM measurements found that the Si/SiO_x core−shell structure of the nanoparticles was not preserved after sintering, and the sintered material consists of two different regions: nanocrystalline regions and amorphous regions (Figure 2a). In the case of the 4 h-oxidation sample,

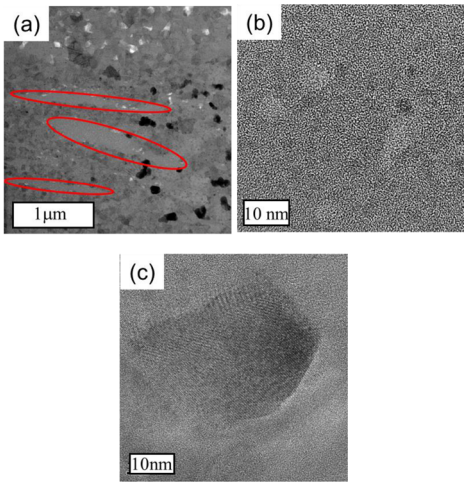

Figure 2. (a) TEM image of the 4 h-oxidation sample, which consists of nanocrystalline Si region and amorphous Si oxide region (the part circled in red). High-resolution TEM of (b) the amorphous oxide region and (c) the nanocrystalline regions.

the size of the amorphous region was in the order of a micrometer, and its area fraction was about 30%. The fraction was small enough to geometrically percolate the nanocrystalline regions. The EDS analysis identified the chemical composition of the amorphous region to be SiO_x (Figure 2b) and the atomic composition percentage of oxygen is about 25%.

The estimated volume fraction of the amorphous region roughly matches that of the oxide shell of the nanoparticle. It is likely that the segregation of the amorphous regions from the nanocrystalline regions is caused by the viscous flow driven by surface tension force between SiO_x and Si during the sintering. It is known in sintering of silica[24,25] that, as temperature exceeds the glass transition temperature, the viscosity of the amorphous oxide becomes small enough to flow, and the amorphous oxide agglomerates to minimize the surface area. Therefore, we expect the fraction of the amorphous region to scale with the relative thickness of the oxide shell, and thus the oxidation time.

The TEM images from the nanocrystalline regions (Figure 2c) show that significant grain growth takes place during sintering. The average grain size is about 30 nm, which agrees with that extracted from the SAXS measurements. In silicon, most of the contribution to electrical conductivity comes from electrons with mean free paths less than 20 nm even at 127 °C,[26] and thus 30 nm is an appropriate size to reduce lattice thermal conductivity while retaining electrical conductivity. The EDS analysis shows that there are also small amount of oxide precipitates in the nanocrystalline regions. They are commonly seen in the Czochralski process and formed due to the difference between the solubility for oxygen in silicon at room temperature and the melting point. The level of other impurities such as chloride and metal was less than 2%.

Figure 3a shows the temperature dependence of the electrical conductivity. The electrical conductivity of all the samples except for the 12 h-oxidation sample decreased with increasing temperature from room temperature to 690 °C due to increase in electron−phonon scattering rates, which is a typical trend of degenerately doped semiconductors. In contrast, above 690 °C,

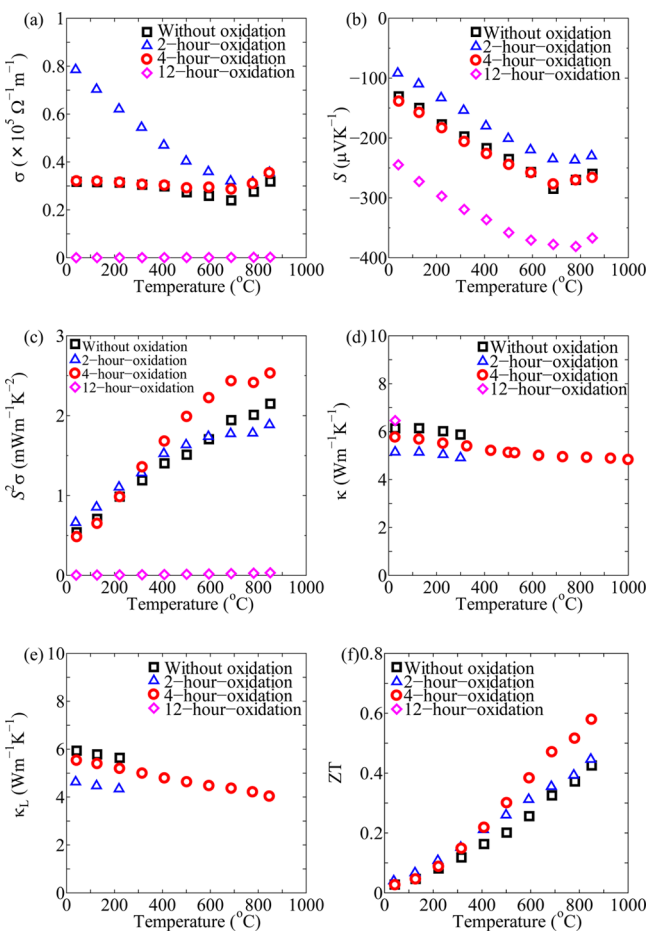

Figure 3. Temperature-dependence of (a) electrical conductivity, (b) Seebeck coefficient, (c) power factor, (d) thermal conductivity, (e) lattice thermal conductivity and (f) ZT of nanostructured bulk Si materials fabricated by sintering of nanoparticles without (black open square) and with oxidization for 2 h (blue open triangle), 4 h (red open circle) and 12 h (pink open diamond).

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the electrical conductivity of all the samples increased with temperature. This, as discussed by Bux et al.,[17] is due to the kinetics of dopant precipitation related to the retrograde solid solubility of phosphorus in silicon. As the temperature increases, the phosphorus trapped in the grain boundaries[27] diffuses back into the silicon grains, carrier concentration increases and electrical conductivity increases. The process is expected to be reversible.

On the other hand, the electrical conductivity of the 12 h-oxidation sample increased with temperature in the entire temperature range. This is the trend seen in disordered materials such as amorphous due to the hopping conduction between localized states. In addition, the electrical conductivity of the 12 h-oxidation sample was 3 orders of magnitude lower than that of the other samples. These observations indicate that, in the case of 12 h-oxidation sample, the nanocrystalline region is no longer geometrically percolated due to the increase in the fraction of the amorphous oxide region.

The carrier concentration n of the samples without oxidation and with 4 h oxidation at room-temperature, obtained by Hall-effect measurement, decreased to about half compared with that of the as-synthesized nanoparticles and 2 h-oxidation sample. The EDS analysis indicates that this could be due to the trapping of phosphorus in the grain boundaries, which is electrically inactive. This trapping is caused by sintering at high temperature or for a long time, which leads not only to the higher density and healing of defects but also to diffusion of the impurities, which tends to segregate to the grain boundaries.

The carrier mobility of the sample without oxidation was 13% of that of bulk Si with the same carrier concentration as the as-synthesized nanoparticles. One of the reasons for the reduction is that charge carriers are scattered by a potential barrier created by charges trapped on the grain boundaries, in addition to the dangling bonds and residual chloride that create localized states and can trap charge carriers. Similarly, the carrier mobility of the 4 h-oxidation sample became 25% of that of bulk Si due to the additional incorporation of amorphous oxide region. Note that containing even a small amount of impurities reduce the carrier mobility. For example, the carrier mobility of the sample without impurities in Claudio et al.,[20] 61 $cm^2\ V^{-1}\ s^{-1}$, is much higher than that of the sample containing a small amount of impurities in Bux et al.[17] and Schierning et al.[19] Note that the value of the carrier mobility of the 4 h-oxidation sample, 18.5 $cm^2\ V^{-1}\ s^{-1}$, is close to that of the optimized sample in Bux et al.[17] and Schierning et al.,[19] despite the presence of the amorphous oxide region of volume fraction of as much as 30 vol %, attributed here to the geometrical percolation of the nanocrystalline region.

Figure 3b shows that all the samples exhibit negative Seebeck coefficient, and thus are n-type semiconductors, over the entire temperature range. The absolute value of Seebeck coefficient of all the samples increased with temperature between room temperature and 690 °C and decreased above 690 °C, which is an opposite tend from that of electrical conductivity. As for the sample dependence, the value is the smallest for 2 h-oxidation and larger in the cases without oxidation and with longer oxidation time.

The absolute value of Seebeck coefficient is anticorrelated with that of the carrier concentration (Table 1) and the electrical conductivity. This trade-off makes the variation in the power factor (Figure 3c) small in the small temperature regime. However, the 4 h-oxidation sample shows significantly better power factor in the high temperature regime.

Figure 3d shows that the thermal conductivity of all the samples is 5−6 W $m^{-1}\ K^{-1}$ and reduced to less than 5% compared to that of bulk Si at room temperature. In the case of the 4 h-oxidation sample, thermal conductivity slightly decreased with temperature to 4.8 W $m^{-1}\ K^{-1}$ at 1000 °C. The value is comparable to that of SiGe.[10] The leading mechanism of the reduction is expected to be the phonons scattering at the grain boundaries in the nanocrystalline part.

To gain quantitative sense to the reduction, we have calculated the lattice thermal conductivity in highly doped Si nanocrystalline materials at room temperature, by viewing lattice heat conduction in terms of Boltzmann transport of phonons:

$$\kappa = \frac{1}{3}\sum_{k,s} C_{v_{k,s}} {v_{k,s}}^2 \tau_{k,s}$$

Here, C_v is the phonon specific heat, v is the phonon group velocity and τ is the phonon relaxation time. The relaxation time is obtained using Matthiessens's rule:

$$\frac{1}{\tau_{k,s}} = \frac{1}{\tau_{\mathrm{ph}_{k,s}}} + B{\omega_{k,s}}^4 + \frac{v_{k,s}}{L}$$

where τ_{ph} is the relaxation time for phonon−phonon scattering, ω is the phonon frequency and L is the grain size. The intrinsic phonon transport properties C_v, v and τ_{ph} are determined by the first-principles calculations,[28] and B is determined by fitting the previously measured thermal conductivity of the sample with almost the same carrier concentration as the current sintered samples (1.7×10^{20} cm^{-3}).[29] Note that although the grain size in actual nanocrystalline materials has a distribution, our recent calculations found that the distribution has only negligible effect on thermal conductivity as long as the average size is constant.[30]

Figure 4 shows the calculated grain-size-dependence of lattice thermal conductivity of highly doped Si nanocrystalline at room temperature. The calculation predicts that nanograins with an average size of 30 nm reduces lattice thermal conductivity to 10.8 W $m^{-1}\ K^{-1}$ at room temperature. This is much larger than the measured lattice thermal conductivity of the current samples (Figure 3e), which suggests the significant role of amorphous regions to reduce thermal conductivity. The impact

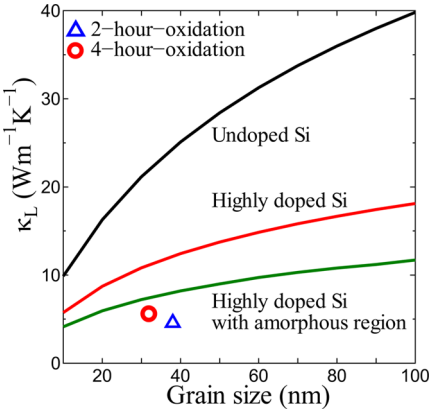

Figure 4. Grain-size-dependence of thermal conductivity at room temperature calculated with first-principles and effective medium theory. The thermal conductivity of highly doped Si with the grain size of 30 nm is 10.8 W $m^{-1}\ K^{-1}$.

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of the amorphous region can be estimated by adopting the effective medium theory, which is widely used to predict effective thermal conductivity of composites.[31] The thermal conductivity of the hybrid material is expressed as

$$\frac{\kappa_e}{\kappa_h} = \frac{\kappa_p(1+2\alpha) + 2\kappa_h + 2\varphi[\kappa_p(1-\alpha) - \kappa_h]}{\kappa_p(1+2\alpha) + 2\kappa_h - \varphi[\kappa_p(1-\alpha) - \kappa_h]}$$

where κ_e is the effective thermal conductivity of the hybrid material, κ_h is thermal conductivity of highly doped Si nanocrystalline materials as mentioned above, κ_p is thermal conductivity of bulk SiO_2,[32] φ is the volume fraction of SiO_x and α is a dimensionless parameter defined as $\alpha = r_{TBR}/(d/2)$. Here, $d = 1$ μm is the diameter of SiO_x and $r_{TBR} = R\kappa_h$, where $R = 2.3 \times 10^{-9}$ m^2 K W^{-1} is the thermal boundary resistance between Si and SiO_2.[33] The calculation (Figure 4) predicted the composite of highly doped Si nanograin with an average size of 30 nm and amorphous region with an average size of 1 μm of volume fraction of 30 vol % reduces lattice thermal conductivity to 7.2 W m^{-1} K^{-1} at room temperature, which agrees with the experimental data.

Figure 3f shows the temperature dependence of ZT. Here, ZT of the samples without oxidation and with 2 h oxidation above 300 °C were determined by using thermal conductivity calculated by extrapolating the data from room temperature to 300 °C, assuming the same linear temperature-dependence as in the 4 h-oxidation case. The 4 h-oxidation sample exhibits the best overall figure of merit, and ZT reaches as high as 0.58 at 850 °C. The 4 h-oxidation sample performs better than the others particularly at high temperatures reflecting the difference in the power factor (Figure 3c).

Figure 5 shows the comparison of the thermoelectric properties between this work and the previous works.[17,19,20,34] The electrical conductivity in this work is lower than those in previous works for the entire temperature range. Note that the difference between this work and Bux et al.[17] comes from the difference in the carrier concentrations, and the mobility is almost the same. On the other hand, current work realizes a larger Seebeck coefficient than the previous works due to the lowest carrier concentration. The resulting power factor in this work is smaller than that in the previous works although it is comparable to that of Bux et al.[17] However, this is greatly compensated by the very low thermal conductivity in this work, and as a result, the ZT at 850 °C of the sample in this work is 25% higher than the best reported value for silicon thermoelectrics using PECVD.[19,20] In addition, the ZT up to 600 °C in this work is equivalent to the best reported value for bulk Si thermoelectrics.[17] Moreover, by realizing lower thermal conductivity, the material cost efficiency has been greatly enhanced.

CONCLUSIONS

Nanostructured bulk Si thermoelectrics were fabricated using plasma sintering of nanoparticles obtained from PECVD. The structural characterization using TEM, EDS and SAXS shows the samples consist of the nanocrystalline silicon region with the average grain size of about 30 nm and the amorphous Si oxide region. Although the carrier concentration of the samples is lower than that of the as-synthesized nanoparticles, the samples with moderate oxidization show reasonable carrier mobility close to that of the optimized samples in Bux et al.[17] and Schierning et al.[19] due to the geometrical percolation of the nanocrystalline region. The composite of the nanocrystalline

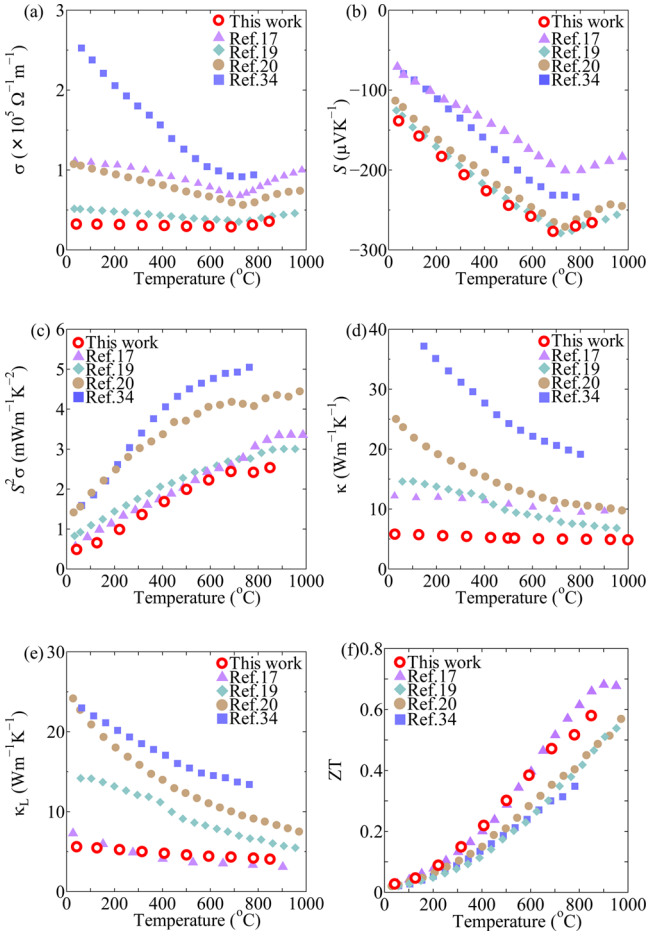

Figure 5. Temperature dependence of (a) electrical conductivity, (b) Seebeck coefficient, (c) power factor, (d) thermal conductivity, (e) lattice thermal conductivity and (f) ZT of nanostructured bulk Si fabricated by sintering of nanoparticles oxidized for 4 h (red open circle) compared with those of previous works (full triangle,[17] full diamond,[19] full circle,[20] full square[34]).

and the amorphous oxide regions reduces thermal conductivity to as low as 5−6 W m^{-1} K^{-1}, which is comparable to that of SiGe. As a result, ZT at 850 °C of the sample in this work is 25% higher than the best reported value for Si thermoelectrics using PECVD.[19,20] In addition, the ZT up to 600 °C in this work is equivalent to the best reported value for bulk silicon thermoelectrics.[17] Lowering thermal conductivity also greatly enhanced the material cost efficiency.

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Notes

The authors declare no competing financial interest.

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